A MATHEMATICAL MODEL FOR POWER MOSFET CAPACITANCES

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Abstract

A mathematically based model for power MOSFET capacitances offers both accuracy and speed for circuit simulation applications. Expressions for the MOSFET capacitances $C_{gd}(v)$, $C_{gs}(v)$ and $C_{ds}(v)$ are derived from a simplified physical model and implemented on the Saber simulator. Data obtained from 60V power MOSFETs are used for comparison.

1.0 Introduction

Numerous MOSFET models have been developed in the past decade [8] to replace the generic or standard low voltage MOSFET model in SPICE. Most of these models incorporate the generic SPICE MOSFET model within a subcircuit of additional passive and active elements. However, such subcircuit models are limited in flexibility and can be slow to simulate.

The wide swings of capacitance with terminal voltage typical of power MOSFETs make simulations of MOSFET waveforms difficult at switching frequencies even as low as 10 kHz. Simple power MOSFET models [1-3] assume constant gate-source capacitance and a 1-step or 2-step gate-drain capacitance. A major shortcoming of such models is inaccurate modeling of the capacitance swings in both the gate-drain and gate-source interfaces. A more accurate approach is to utilize a power series expression for C_{gd} [6] but this becomes complex to set up and computation-intensive. The most accurate subcircuit model uses a special MOS capacitor available in a particular version of SPICE [7]. A review of existing power MOSFET models [3,8] indicates the need for precise expressions of MOSFET capacitances as functions of terminal voltages.

In this paper the capacitance-voltage equations are derived and then directly implemented into a power MOSFET model as an alternative to the sub-circuit approach. The goal is to develop a fast and simple power MOSFET model whose parameters depend on easily measured external device properties rather than internal phenomena. By deriving equations directly from device physics one obtains accurate functioning over a wide range of circuit conditions and device types.

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The objective of this paper is to mathematically describe the capacitance-voltage characteristics of the interelectrode capacitances in the power MOSFET. The internal charge conditions which determine the capacitances for different operating states are presented in Section 2. In Section 3, experimental three terminal capacitance data are compared with simulated results, followed in Section 4 by a brief description of how parameters were determined.

2.0 The Seven Operating States of the Power MOSFET

All three terminal capacitances C_{gd} (V_{GD}), C_{gs} (V_{GS}) and $C_{ds}(V_{DS})$ must be modeled together as one system since the internal mobile charges which give rise to the capacitances interact with each other and are shared among the three terminal capacitances. The observed gate capacitance variations are due to changes in charge location under the gate in both the n^- drain and p-body regions. Each of these two regions can be separately in either **accumulation, depletion** or **inversion** state. When one considers all possible combinations of these three states for both regions under the gate, one obtains the nine possible operating states shown in Table 1. Each state represents a specific arrangement of the internal stored charge under the gate of the power MOSFET.

Table 1. The seven operating states of the power MOSFET

MOSFET p-body States as functions of V_{GS}

MOSFET n-drain States as functions of V_{GD}	Inversion	Depletion	Accumulation
Accumulation	ON-State $q_{GS} = Q_{BI} + Q_{BDC}$ $q_{GD} = Q_{DA}$ $q_{DS} = Q_J$	Reverse State $q_{GS} = Q_{BD}$ $q_{GD} = Q_{DA}$ $q_{DS} = Q_J$	
Depletion	Active State $q_{GS} = Q_{BI} + Q_{BDC}$ $q_{GD} = Q_{DD}$ $q_{DS} = Q_J$	OFF-1 ($V_{GS} > V_{GBfb}$) $q_{GS} = Q_{BD}$ $q_{GD} = Q_{DD}$ $q_{DS} = Q_J$	OFF-2 (High V_{DS}) $q_{GS} = Q_{BA}$ $q_{GD} = Q_{DD}$ $q_{DS} = Q_J$
Inversion		OFF-4 (Low V_{DS}) $q_{GS} = Q_{BD}$ $q_{GD} = Q_{DI} + Q_{DDI}$ $q_{DS} = Q_J$	OFF-3 (Low V_{DS}) $q_{GS} = Q_{BA} + Q_{DI} + Q_{DDI}$ $q_{GD} = 0$ $q_{DS} = Q_J + Q_{DDI}$
	$V_{GS} = V_T$	$V_{GS} = V_{GBfb}$	$V_{GD} = V_{GD}(V_{GS})$

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Closer examination indicates that only seven of the nine states are possible for a practical power MOSFET. Six are quasi-static states and the seventh, the OFF-4 State, is a dynamic state involving charge and discharge of an isolated inversion layer of holes trapped at the surface of the n⁻ drain region. The remaining two states: the simultaneous accumulation or inversion of mobile carriers in both the n⁻ drain and p-body regions, are either impossible or destructive to a power MOSFET. The boundaries which separate one quasi-static state from another are the following terminal voltages:

1) V_T - Gate-Source Threshold voltage or Turn-on voltage of a power MOSFET.
2) V_{GBfb} - Gate-Body flat-band voltage for the p-body region.
3) V_{GDfb} - Gate-Drain flat-band voltage for the n⁻drain region.
4) $V_{GDI}(V_{GS})$ - Gate-Drain voltage at which inversion occurs at the n⁻ drain and gate insulator interface.

The first three are constants, but the gate-drain inversion boundary $V_{GDI}(V_{GS})$ shifts with changes in V_{GS} or V_{DS} bias. At a higher drain-source voltage, a more negative (for an n-channel MOSFET) gate-source bias voltage is required to induce drain region inversion.

The charge symbols shown in each state of Table 1 are defined as:

Q_{BI} - Body-Inversion charge
Q_{BD} - Body-Depletion charge
Q_{BDC} - Body-Depletion constant charge (inversion state)
Q_{BA} - Body-Accumulation charge
Q_{DI} - Drain-Inversion charge
Q_{DD} - Drain-Depletion charge in OFF-1, OFF-2
Q_{DDI} - Drain-Depletion charge in OFF-3, OFF-4 (inversion)
Q_{DA} - Drain-Accumulation charge
Q_J - Junction depletion charge of the Body-Drain diode

These charges are functions of terminal voltages and their equations are derived using the set of simplifying assumptions commonly known as the **Delta-Depletion Approximation** [9]:

a. The depletion region has a uniform charge density containing only ionized atoms.
b. The charges on the gate and interface are contained in extremely thin layers.
c. The charge density is constant along the length of the inversion layer.

Although previous power MOSFET models have assumed that the p-body is heavily enough doped to have a constant gate-body capacitance, our measurements indicate that the gate p-body interface contributes a 3:1 variation in C_{gs} with voltage. Thus, the complete delta-depletion model must be applied to both the n⁻ drain and p-body regions as diagrammed in Figure 1.

To individually identify the currents for $C_{gd}(v)$ and $C_{gs}(v)$, the total gate charge $q_G(v)$ is separated into $q_{GS}(v)$ for current through $C_{gs}(v)$ and $q_{GD}(v)$ for current through $C_{gd}(v)$. Furthermore, the highly nonlinear $C_{ds}(v)$ of the body-drain junction is determined by the charge q_{DS} which depends on both the junction depletion charge $Q_J(V_{DS})$, and the inversion charge Q_{DDI} in the n⁻ drain region. From a circuit perspective, the gate current is the rate of change of the total gate charge $\frac{d(q_{GS} + q_{GD})}{dt}$ and the drain current is $\frac{d(q_{DS} - q_{GD})}{dt}$. For each of the seven practical states in Table 1, the charge transitions are described next, following the order which occurs as a MOSFET turns off.

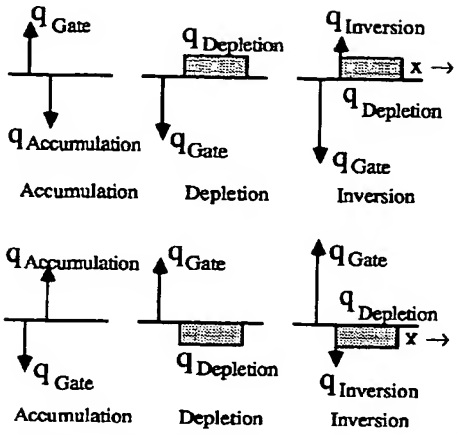

Figure 1. Three possible surface charge states for the n-type drain region (above) and the p-type body region (below)

The **ON-State** of the MOSFET corresponds to accumulation in the n⁻ surface region, with $V_{GD} \geq V_{GDfb}$; and inversion at the p-body and gate interface, with $V_{GS} \geq V_T$. The internal charge equations are:

$$q_{GS} = Q_{BI} + Q_{BDC} \quad (1)$$

$$q_{GD} = Q_{DA} \quad (2)$$

$$q_{DS} = Q_J \quad (3)$$

Here, Q_{BDC} is a constant charge which does not affect the current through $C_{gs}(v)$. It is needed to ensure charge continuity for $q_{GS}(v)$ in transition between depletion and inversion. The physical location of these charges is shown in Figure 2.

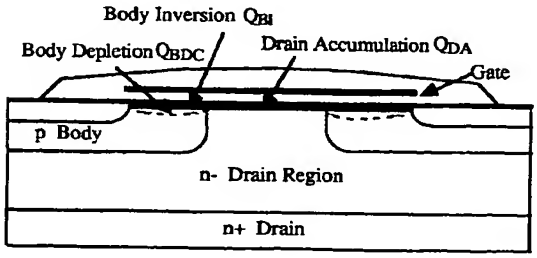

Figure 2. MOSFET in the ON-State showing the physical locations of the charges Q_{BI}, Q_{BDC}, Q_{DA}

The **Active State** of the MOSFET occurs when the p-body is already in inversion, but a relatively high V_{DS} exists which keeps the n⁻ drain in depletion, with $V_{GD} < V_{GDfb}$. Figure 3 shows that during this quasi-static state, charge distribution in the p-body is unchanged while q_{GD} becomes:

$$q_{GD} = Q_{DD} \quad (4)$$

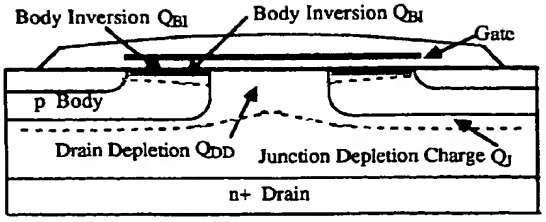

Figure 3. MOSFET in the Active State showing gate-drain depletion Q_{DD} as well as Q_{BI} and Q_{BDC}

In the **OFF-1** State, both the n^- drain and p-body regions are depleted of mobile carriers, corresponding to the earliest stage of the power MOSFET's OFF condition. This state of operation is defined by $V_{GBfb} < V_{GS} < V_T$ and $V_{GD} < V_{GDfb}$. Here, Figure 4 shows that the drain depletion region remains unchanged and

$$q_{GS} = Q_{BD} \quad (5)$$

$$q_{GD} = Q_{DD} \quad (6)$$

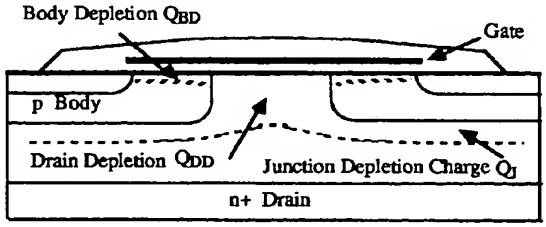

Figure 4. MOSFET in the OFF-1 State showing Q_{BD} and Q_{DD}.

As the gate voltage swings further negative, accumulation of hole carriers in the p-body begins to occur when $V_{GS} \leq V_{GBfb}$. If V_{DS} is high, such that $V_{GD} > V_{GDI}(V_{GS})$, then the relatively negative potential of Q_{BA} makes inversion at the n^- drain surface impossible as shown in Figure 5. We call this the **OFF-2** State of operation. Here q_{DS} and q_{GD} are the same as those in OFF-1, but

$$q_{GS} = Q_{BA} \quad (7)$$

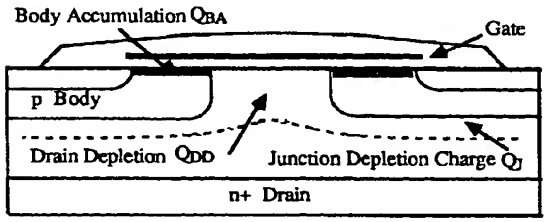

Figure 5. MOSFET in the OFF-2 State showing Q_{BA} and Q_{DD}.

If V_{DS} is low and $V_{GS} \leq V_{GBfb}$, then an inversion layer of holes will form at the n^- drain surface when $V_{GD} \geq V_{GDI}(V_{GS})$. Once this inversion layer forms, the gate-drain is effectively shielded [7] and $C_{gd}(v)$ drops to zero. Figure 6 shows how this shielding effect also causes a "short circuit" of the n^- inversion region across the p-body to the source resulting in an increase of $C_{ds}(v)$ due to connection of the depletion charge (Q_{DDI}) across the drain-source electrodes. This quasi-static state is named **OFF-3**, where Q_{DDI} is now a function only of V_{DS}.

$$q_{GS} = Q_{BA} + Q_{DI} + Q_{DDI} \quad (8)$$

$$q_{GD} = 0 \quad (9)$$

$$q_{DS} = Q_J + Q_{DDI} \quad (10)$$

Note that inversion in the n^- region can occur only after accumulation has taken place along the surface of the p-body region.

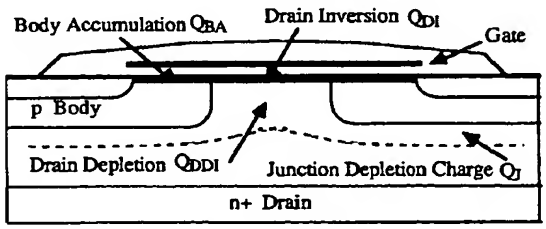

Figure 6. MOSFET in the OFF-3 State showing Q_{BA}, Q_{DI}, and Q_{DDI}.

In contrast to the other states which are all quasi-static, the **OFF-4** is a dynamic state in which the p-body region is in depletion and can trap a layer of inversion charge along the surface of the n^- drain as shown in Figure 7. This trapped charge will relax to its steady-state value in a time constant corresponding to the surface lifetime τ. The OFF-4 state occurs during MOSFET turn-off and turn-on at low drain voltages V_{DS}. With $Q_{DI}(t_0)$ the initial inversion charge and Q_{DI} the steady-state value, the charge equations are

$$q_{GS} = Q_{BD} \quad (11)$$

$$q_{GD} = Q_{DDI} + Q_{DI}(t_0)\exp(-\frac{t}{\tau}) + Q_{DI}[1 - \exp(-\frac{t-t_0}{\tau})] \quad (12)$$

$$q_{DS} = Q_J \quad (13)$$

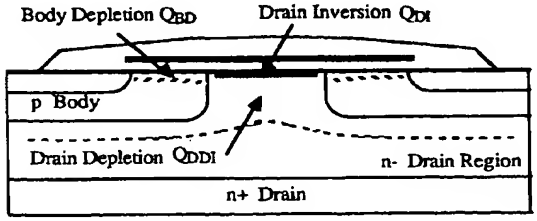

Figure 7. MOSFET in the OFF-4 State showing Drain Inversion Q_{DDI} with Body Depletion Q_{BD}

No attempt has been made to include the dynamic characteristics of the OFF-4 state in the computer model. Instead this state is modeled and implemented on the simulator as a quasi-static state, assuming the trapped charge instantly relaxes to its steady-state value ($\tau = 0$ in (12)). The dynamic effect is not considered significant enough now to warrant the additional complexity in the model.

In the **Reverse State**, the p-body has yet to achieve inversion and remains in depletion. Thus, $V_{GS} < V_T$. However, a low V_{DS} allows the n⁻ drain surface to reach accumulation where $V_{GD} \geq V_{GDfb}$.

$$q_{GS} = Q_{BD} \qquad (14)$$

Here, q_{GD} and q_{DS} are the same as Eq.(2) and (3) respectively. This state occurs during resonant switching where $v_{DS}(t)$ reverses polarity while the power MOSFET current $i_{DS}(t)$ is zero.

The complete set of power MOSFET charge equations as functions of the terminal voltages V_{GD}, V_{GS}, V_{DS} are derived in the Appendix. The charge equations are implemented in a three-terminal capacitance model, called a template, in the Saber simulator. The template reinitializes the simulator whenever the simulation crosses a boundary between two of the seven operating states of Table I. The capacitive currents at the three device terminals are determined by taking the derivatives of these charge expressions.

3.0 Experimental Data and Simulation Results

Capacitance-voltage measurements on a P8NO8 Power MOSFET were taken over a complete range of V_{DS} and off-state V_{GS} bias conditions. The three interelectrode capacitances $C_{gd}(v)$, $C_{gs}(v)$ and $C_{ds}(v)$ were measured separately using the three terminal measurement technique shown in the schematic in Figure 8.

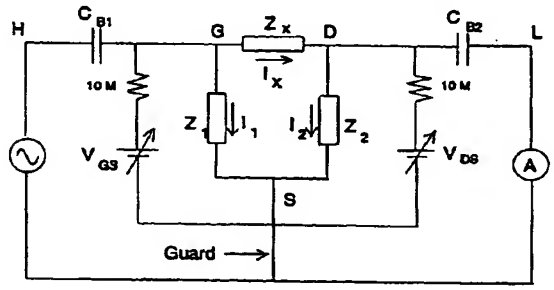

Figure 8. Circuit for measuring $C_{gd}(V_{GS},V_{DS})$

The effects of parallel impedances are eliminated by using the guard terminal which functions as the circuit common. The guard terminal is electrically different from the ground which is connected directly to the instrument chassis.

With the guard properly connected the measurement of the "unknown" capacitance or impedance Z_X is unaffected, because Z_X is calculated using current I_X. In Figure 8, the current I_2 is negligible compared to I_X because the internal resistance of the ammeter is very low in comparison to the impedance Z_2.

Data on $C_{ds}(v)$ is shown in Figure 9. For a constant V_{GS} bias of -5V on the MOSFET gate, a decreasing V_{DS} moves the n⁻ drain region from depletion (OFF-2) to inversion (OFF-3). At the transition the drain depletion charge Q_{DDI} is added to the drain-source junction depletion charge Q_J resulting in the abrupt increase in C_{ds}. The simulated $C_{ds}(v)$ plot shows the same transition as an abrupt jump in the capacitance value at the point where inversion occurs. For V_{GS} = 10V and below, both the measured and simulated C_{ds} are shown to operate in the OFF-3 state; while at a low V_{GS} of 0V, the drain-source capacitance operates only in the OFF-1 state. The gate-body flatband voltage (V_{GBfb}) has been set to -2V for all the simulations. The abrupt jump in capacitance value as shown for V_{GS} = -5V is a result of the delta-depletion approximation assumed for the capacitance model.

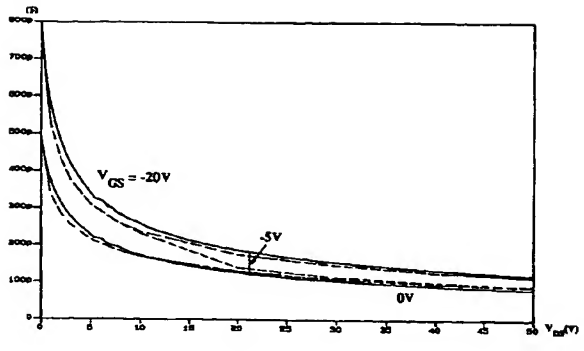

Figure 9. Measured C_{ds} (dash) and simulated C_{ds} (solid) versus V_{DS} for V_{GS} = 0V, -5V, -20V. The arrow shows the transition from OFF-2 to OFF-3 as V_{DS} decreases.

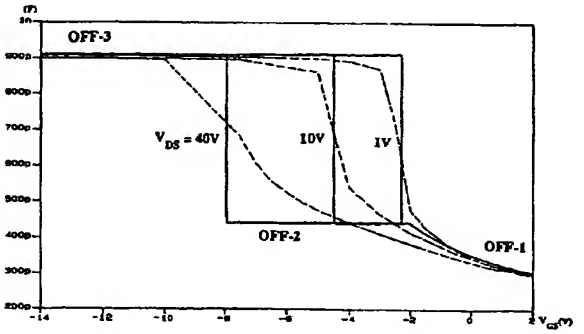

Figure 10. Plots of $C_{gs}(v_{GS})$ for V_{DS} = 1V, 10V, 40V. Measured (dashed) and simulated (solid).

Data on $C_{gs}(v)$ is shown in Figure 10 where for $V_T > V_{GS} > V_{GBfb}$, the n⁻ drain region is depleted of mobile carriers (OFF-1). As V_{GS} becomes more negative, inversion takes place along the n⁻ drain interface with the gate, causing the effective area of C_{gs} and therefore, its magnitude, to increase. As V_{DS} increases, inversion in the drain occurs at more negative V_{GS} values. The simulation results show that the curvature of the body-depletion capacitance is unchanged for all V_{DS} bias in contrast to the varying curvature of the measured body-depletion capacitance. For $V_{GS} < V_{GBfb}$ and $V_{GD} \leq V_{GDI}(V_{GS})$, the model gives a constant OFF-2 state capacitance (flat after the depletion-accumulation boundary at V_{GS} = -2V which again is not observed in the measured data. These descrepancies are most likely due to the use of the delta-depletion model in the simulation.

Alternatively, if drain inversion occurs prior to $V_{GS} \leq V_{GBfb}$, the capacitance $C_{gs}(v)$ moves from OFF-3 to OFF-1 via OFF-4 as V_{GS} is increased. In the model, the OFF-4 state is modeled as a quasi-static state which produces an abrupt rise in capacitance during the OFF-4 state as shown in Figure 11. Since this is a dynamic state, high frequency capacitance measurements will not show the capacitance peak in Figure 11. However in an actual MOSFET switching transient, the charge associated with the large OFF-4

capacitance will be transferred as the device moves from the dynamic OFF-4 into the quasi-static OFF-1 or OFF-3 state. For this reason, the OFF-4 state is important to retain in the model.

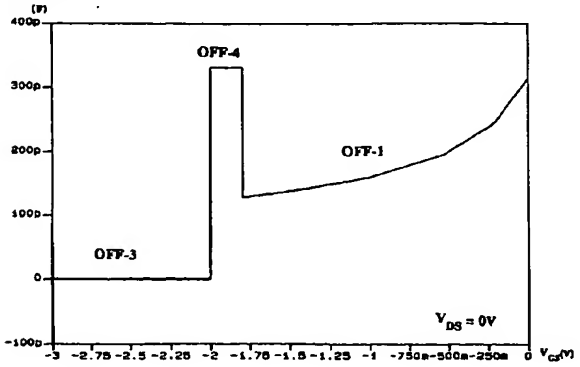

Figure 11. Simulated $C_{gd}(v_{GS})$ showing OFF-4 state for V_{DS} =0V

With $V_{GS} = 3V \geq V_T$, the $C_{gd}(v_{GD})$ plot goes from the ON-state to the Active-state of MOSFET operation as shown in Figure 12. The simulated $C_{gd}(v_{GD})$ exhibits a constant capacitance corresponding to C_{gdon} in the ON-state for low V_{DS}, and then a decreasing depletion capacitance in the Active-state for $V_{DS} > V_{GS} - V_{GDfb}$. For V_{GS} = -3V, an inversion layer at the n^- drain surface forms during $V_{GS} - V_{DS} \geq V_{GDI}(V_{GS})$ which "shields" the gate-drain depletion charge from the gate-drain interface making $C_{gd}(v)$ effectively drop to zero. The simulated $C_{gd}(v)$ plot again shows the transition between OFF-3 and OFF-2 states as an abrupt jump in capacitance value as a result of the delta-depletion approximation. For $V_{GS} - V_{DS} < V_{GDI}(V_{GS})$, the $C_{gd}(v)$ depletion capacitance decreases as V_{DS} is increased.

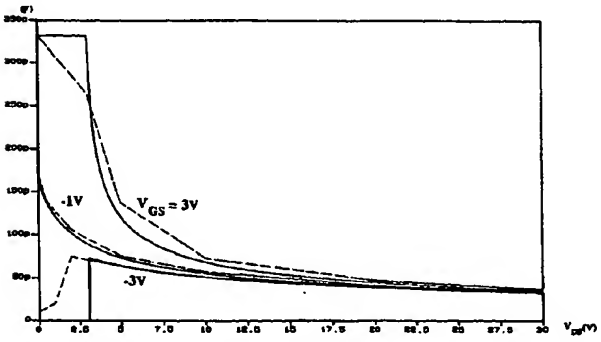

Figure 12. Plot of $C_{gd}(v_{DS})$ for V_{GS} = 3V, -1V, -3V. The measured plot is dashed; the simulated solid.

4.0 Parameter Determination

The set of MOSFET charge equations in in the Appendix contain the nine parameters given in Table 2. This set of parameters are required to characterize all three MOSFET interelectrode capacitances.

Table 2. Parameters used in charge equations

Parameter	Value in simulation	Definition
C_{gdon}	332 pF	Constant, ON-State value of the gate-drain capacitance
C_{gson}	442 pF	Constant, ON-State value of the gate-source capacitance
V_T	2.2 V	Threshold voltages for the p-body
V_{TD}	-0.2 V	Threshold voltages for the n- drain
V_{GBfb}	-2.0 V	Gate-Body flat-band voltage for the p-body region.
V_{GDfb}	0 V	Gate-Drain flat-band voltage for the n-drain region
V_{bD}	0.8 V	Zero-bias built-in voltage between the drain and surface during inversion.
V_{bA}	0.8 V	Zero-biased built-in voltage between the p-body and surface during inversion
C_{jo}	492 pF	Junction capacitance of the drain-source interface

Five of the seven parameters C_{gdon}, C_{gson}, V_T, V_{GBfb} and C_{jo} were extracted from the measured capacitance data. Two parameters V_{GDfb} and V_{TD} were determined by curve-fitting the simulated capacitance curves with the measured ones. The two built-in voltages V_{bA} and V_{bD} were simply assumed to be equal to 0.8 V.

A more practical and direct way to determine the MOSFET parameters is needed. For example, many of the capacitance parameters may be determined from the gate-charge plots in MOSFET data books.

5.0 Discussion

The use of the delta-depletion approximation to model the MOSFET capacitances greatly simplifies the modeling of the internal charges within the accumulation, depletion, and inversion states. However, the complete model with seven operating states becomes complex.

Nevertheless, the relative accuracy of the capacitance model in simulating the real capacitances validates the mathematical equations and the assumptions made in creating the model. Furthermore, the total CPU time on an H-P 3000 for a complete capacitance sweep ranged from 5 to 30 seconds.

The same delta-depletion concept introduces abrupt changes to Q_{GS} and Q_{GD} during inversion of the p-body and the n^- drain as demonstrated by the abrupt jump in the capacitance value occurring at the point of inversion. These charge and capacitance discontinuities are a major drawback of this implementation. They can make simulation difficult and frequently cause simulation failures.

Perhaps, this limitation of the delta-depletion model can be overcome by a more gradual modeling of the transition between depletion and inversion.

Or alternatively, such a model may be judged too complex for practical use in a circuit simulator, and simplification should be considered. For example, if the 3:1 variation of $C_{gs}(v)$ is omitted, the complexity of the model can be decreased almost in half.

6.0 Conclusions

A comprehensive charge-based model for the power MOSFET capacitances is derived and implemented on the Saber simulator. Comparison of the simulated capacitances with measured data verifies the validity of the capacitance model.

However, the power MOSFET is a deceptively complex device to model accurately, and further work is required to make a practical model for circuit simulation purposes. Still needed are:

1) experimental clarification of the critical performance features necessary to include in a power MOSFET model.
2) a simple and direct parameter determination method.
3) an improvement to the modeling of capacitance transitions.

7.0 References

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Appendix: Derivation of the Q(v) Charge Expressions

The symbols used in this section are:

C_{gdon}, C_{gson}	- Constant, ON-State values of the gate-drain and gate-source capacitances.
V_T, V_{TD}	- Threshold voltage for the p-body and the n- drain.
N_A, N_D	- doping concentration of both p-type and n-type semiconductor.
X_{dB}, X_{dD}	- depth of the depletion in p-body and n- drain.
A	- area of active region.
V_{NA}, V_{ND}	- constants (with units of voltage) representing fixed physical quantities for the p-type and n-type semiconductor.
V_{bD}	- zero-bias built in voltage between the drain and surface during inversion.
V_{bA}	- zero-biased built in voltage between the p-body and surface during inversion.
C_{jo}	- junction capacitance of the drain-source interface.

The charges Q_{BA}, Q_{BI}, Q_{DA} are simple functions of the terminal voltages as can be seen from Figure 1:

$$Q_{BI} = -C_{gson}(V_{GS} - V_T) \quad (15)$$

$$Q_{BA} = -C_{gson}(V_{GS} - V_{GBfb}) \quad (16)$$

$$Q_{DA} = -C_{gdon}(V_{GD} - V_{GDfb}) \quad (17)$$

All of the above charges go to zero as the voltage approaches the boundary value.

Following the delta-depletion approximation, the n-drain region depletion charge $q_{Depletion}$ of Figure 1a can be expressed as:

$$q_{Depletion} = qN_DAX_{dD} = Q_{DD} \quad (18)$$

This charge is related to the terminal voltages by

$$q_{Depletion} = \left[qk_D(V_{DS} + V_{bD})\right]^{\frac{1}{2}} \quad (19)$$

where $k_D = 2\varepsilon_{Si}N_DA^2$.

Next, we want to relate V_{TD}, V_{GBfb} to the physical quantities N_D, ε_{Si}, and C_{ox} of the semiconductor. From the potential equation:

$$V_{TD} - V_{GDfb} = \psi_{ox} + \psi_s \quad (20)$$

where

$$\psi_{ox} = \frac{qN_DX_{dD}A}{C_{gdon}} \quad (21) \quad \text{and} \quad \psi_s = \frac{qN_DX_{dD}^2}{2\varepsilon_{Si}} = V_{bD} \quad (22)$$

Then, Eq. (18), (20), (21) and (22) lead to:

$$V_{TD} - V_{GDfb} = \left(2V_{bD}\right)^{\frac{1}{2}}(2V_{ND})^{\frac{1}{2}} + V_{bD} \quad (23)$$

where $$V_{ND} = \frac{qk_D}{4C_{gdon}^2} \quad (24)$$

Then from Eq. (19) and (24), the depletion charge during inversion at the n- drain surface becomes:

$$Q_{DDI} = C_{gdon}\left[4V_{ND}\left(V_{DS} + V_{bD}\right)\right]^{\frac{1}{2}} \quad (25)$$

Prior to inversion, the depletion charge is a function of V_{GD}. Thus, if we let $V_{DS} = V_{GS} - V_{GD}$,

$$q_{Depletion} = Q_{DD} = -2C_{gdon}V_{ND}\left[1 - \left(1 - \frac{(V_{GD} - V_{GDfb})}{V_{ND}}\right)^{\frac{1}{2}}\right] \quad (26)$$

Similarly for the p-body depletion region:

$$V_T - V_{GBfb} = \left(2V_{bB}\right)^{\frac{1}{2}}(2V_{NA})^{\frac{1}{2}} + V_{bB} \quad (27)$$

$$V_{NA} = \frac{qk_B}{4C_{gson}^2} \quad (28)$$

$$Q_{BD} = 2C_{gson}V_{NA}\left[1 - \left(1 + \frac{(V_{GS} - V_{GBfb})}{V_{NA}}\right)^{\frac{1}{2}}\right] \quad (29)$$

The constant body depletion charge Q_{BDC}, during the inversion of the p-body is given by:

$$Q_{BDC} = 2C_{gson}V_{NA}\left[1 - \left(1 + \frac{(V_T - V_{GBfb})}{V_{NA}}\right)^{\frac{1}{2}}\right] \quad (30)$$

During inversion of the n⁻ drain region, the gate charge associated with the gate-drain interface is

$$q_{GD} = C_{gdon}(V_{GS} - V_{GDfb} + V_{bD}) \quad (31)$$

Since $-q_{GD} = q_{Depletion} + q_{Inversion}$, where $q_{Inversion} = Q_{DI}$,

$$Q_{DI} = -q_{GD} - Q_{DDI}$$
$$= -Cgdon\left((V_{GS} - V_{GDfb} + V_{bD}) + \left[4V_{ND}(V_{DS} + V_{bD})\right]^{\frac{1}{2}}\right) \quad (32)$$

The inversion condition $V_{GDI}(V_{GS})$ for the n⁻ drain region is derived by setting $Q_{DI} = 0$. Then Eq.(29) becomes:

$$V_{GD} = V_{GDI} = V_{GS} + V_{bD} - \frac{1}{4V_{ND}}(V_{GS} - V_{GDfb} + V_{bD})^2 \quad (33)$$

Eq.(30) shows that at higher drain-source voltages, inversion of the n⁻ drain occurs at increasingly negative gate-source voltages.

Finally, the charge associated with the drain-source capacitance is

$$q_{DS} = \frac{C_{jo}V_b\left(1+\frac{V_{DS}}{V_b}\right)^{1-m}}{(1-m)} \quad (34)$$